Amendments to the Claims

The listing of claims will replace all prior versions, and listings of claims in the application.

1. (Currently Amended) An apparatus for conducting bench testing of data fields, comprising:

a memory configured to store a number representative of the number of data fields to be analyzed;

a hardware module~~,~~ coupled, at least indirectly, to the memory and configured to (i) receive an input data stream, (ii) perform a cyclic redundancy ~~check~~ checksum (CRC) ~~analysis of~~ processing on the received data stream, and (iii) produce an output representative of an actual number of received data fields analyzed~~;~~, wherein the input data stream includes synchronization markers defining boundaries of each of the received data fields;

a comparator configured to (i) compare the number stored in memory and the actual number of received data fields for which CRC has been processed and (ii) produce a disabling signal when the actual number matches the ~~required~~ number stored in the memory; and

a detector coupled to the comparator and configured to (i) receive the input data stream and sense ~~sensing a presence of~~ the synchronization markers, (ii) receive the disabling signal, and (iii) disable the module when the disabling signal is received.

2. (Currently Amended) The apparatus of claim 1, wherein the module commences the ~~analysis~~ processing in ~~substantial~~ synchronism with a first of the synchronization markers; and

wherein the module is disabled in substantial synchronism with another of the synchronization markers.

3. (Original) The apparatus of claim 1, wherein the hardware module is configured to receive video pixel data.

4. (Currently Amended) The apparatus of claim 1, wherein the hardware module is configured to receive vertical synchronization ~~pulses~~ markers.

5. (Currently Amended) The apparatus of claim 4, wherein the hardware module is configured to receive ~~the~~ a vertical synchronization marker during video blanking.

6. (Original) The apparatus of claim 1, wherein the memory is a register.

7. (Currently Amended) A method for performing cyclic redundancy checksum (CRC) ~~analysis~~ processing of video data in a bench testing system including a memory and a CRC module coupled, at least indirectly, to the memory, the video data including (i) a number of data fields and (ii) synchronization markers defining boundaries of the data fields, the method comprising:

storing a number in the memory, the number being representative of ~~an amount~~ the number of data fields to be checked; ~~and~~

receiving the ~~particular number of~~ data fields and their associated synchronization markers in the CRC module; and

storing a ~~the~~ number of data fields equal to the number of data fields to be checked, ~~substantially~~ in synchronism with a first synchronization marker associated with a beginning of a first received field of the ~~particular number of~~ data fields.

8. (Currently Amended) The method of claim 7, wherein the CRC module ceases receiving ~~the particular number of~~ data fields in ~~substantial~~ synchronism with a last marker associated with an end of a last of the received fields of the ~~particular~~ number of data fields to be checked.

9. (Currently Amended) An apparatus configured to ~~performe~~ perform cyclic redundancy checksum (CRC) ~~analysis~~ processing of video data, the video data having a plurality of data fields and a synchronization ~~marker~~ markers defining boundaries of each of the data fields , the apparatus comprising:

a memory configured for storing a number, the number being representative of a quantity of data fields to be checked;

a CRC module coupled, at least indirectly, to the memory and configured to receive the ~~particular number of~~ data fields and the synchronization markers ~~associated with the received particular number of data fields~~; ~~and~~

a sensing device coupled to the CRC module and configured to sense the synchronization markers; and

wherein the CRC module commences ~~receiving~~ processing the ~~particular number of~~ data fields ~~substantially~~ in synchronism with a first sensed synchronization marker.

10. (Currently Amended) The apparatus of claim 9, wherein the CRC module ceases processing ~~receiving the particular number of~~ data fields in ~~substantial~~ synchronism with a last sensed synchronization marker.

11. (Original) The apparatus of claim 9, wherein the memory is a register.

12. (Original) The apparatus of claim 9, wherein the apparatus is a video test bench set-up.